CLAIMS

I claim:

1. Electronic circuit of data processing to emulate a logic function. This circuit is characterized the following elements:

a single clock providing representative signals of time unit,

a synchronous programmable logic array processing values per time unit,

a means of state change detection, designated "events" of internal or external values,

a means of programming signals for changing state or directly the events,

a mean of successive scheduled times processing providing, to the logic array, representative scheduled time signals according to the signals provided by the mean of detection or by the mean of programming of events and the signals provided by the clock, the processing mean being adapted to determine scheduled times, at time delayed by programming by the programming mean, to happen function to provided signals by the said mean of detection of the said mean of programming,

the processed operations done by the logic array being the result of successive scheduled times initiated by internal or external state changes, and by a successive scheduled time determination.

2. Electronic circuit according to the claim 1, characterized by the fact that the logic array reproduces the simulator operation has the possibility to be integrated into an electronic circuit, the clock defining time unit being tuned for the reproduction of the simulator.

3. Electronic circuit according to the claim 1, characterized by the fact that the logic array is able to emulate, at real time, a logic function without any logic element emulation.

4. Electronic circuit according to any of claim 1 to 3, characterized by the fact that the logic array consists of internal logic processing cells and peripheral communication cells with the outside of the electronic circuit, the signals provided by the scheduled time processing controlling the operation through at least one internal cell or one peripheral cell.

5. Electronic circuit according the claim 4, characterized by the fact that the cells exchange data through one single group of lines on which is set up an exchange per time unit, the cells being adapted to generate signals, random or programmed events, towards the scheduled time processing unit, the said mean of processing scheduled time providing to each cell a command group.

6. Electronic circuit according to any of claims 1, 4 or 5, characterized by the fact that the cells of internal processing cells are able to process a logic word per time unit.

7. Electronic circuit according to claim 6, characterized by the fact that the internal logic cells are adapted to merge several data group issued of several respective identities and to memorize each merged logic word.

8. Electronic circuit according to claims 4 to 7, characterized by the fact that the peripheral cells are adapted to sample logic words received from the external of the circuit and to generate merged logic words according the communication direction.

9. Electronic circuit according to the claim 5, characterized by the fact that the logic array consists of a specific mean of communication with the outside of the circuit, the logic array setting up memorized logic words adapted to be read or modified by the said specific communication mean.

10. Simulator, characterized by the fact that it consists of an electronic circuit according to any one of claims 1 to 9.

11. Emulator, characterized by the fact that it consists of an electronic circuit according to any one of claims 1 to 9.

12. Electronic circuit according the claim 4, characterized by the fact that a scheduler which needs no scheduled time processing other than delays managed by a register matrix and a conflict detection between scheduled times.

13. Electronic circuit according the claim 12, characterized by the fact that the reading and changing of scheduled times by the said specific communication mean.

14. Electronic circuit according the claim 4, characterized by a logic combination of output datas of internal or peripheral communication cells.